Marina Cheng
Sharon Vizcaíno
CSC270 – HW#3

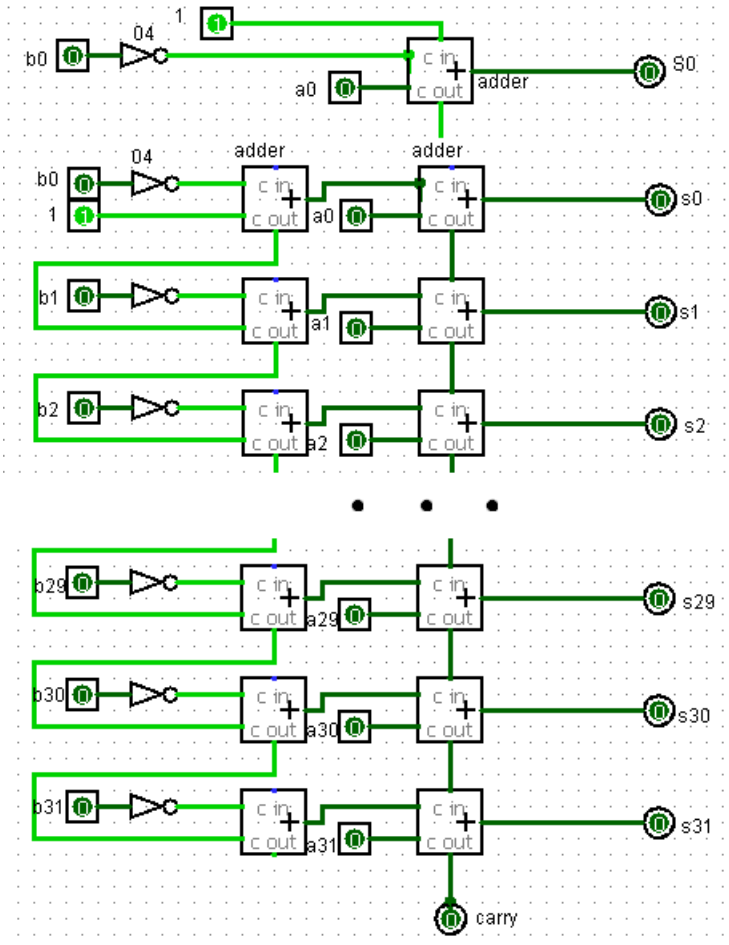
Problem 1

We designed a 32-bit subtraction circuit that will output a-b. a and b are the 2 integers whose bits are shown in the diagram. a is represented by a31…a0, and b is represented by b31…b0

a-b is a plus the 2's complement of b

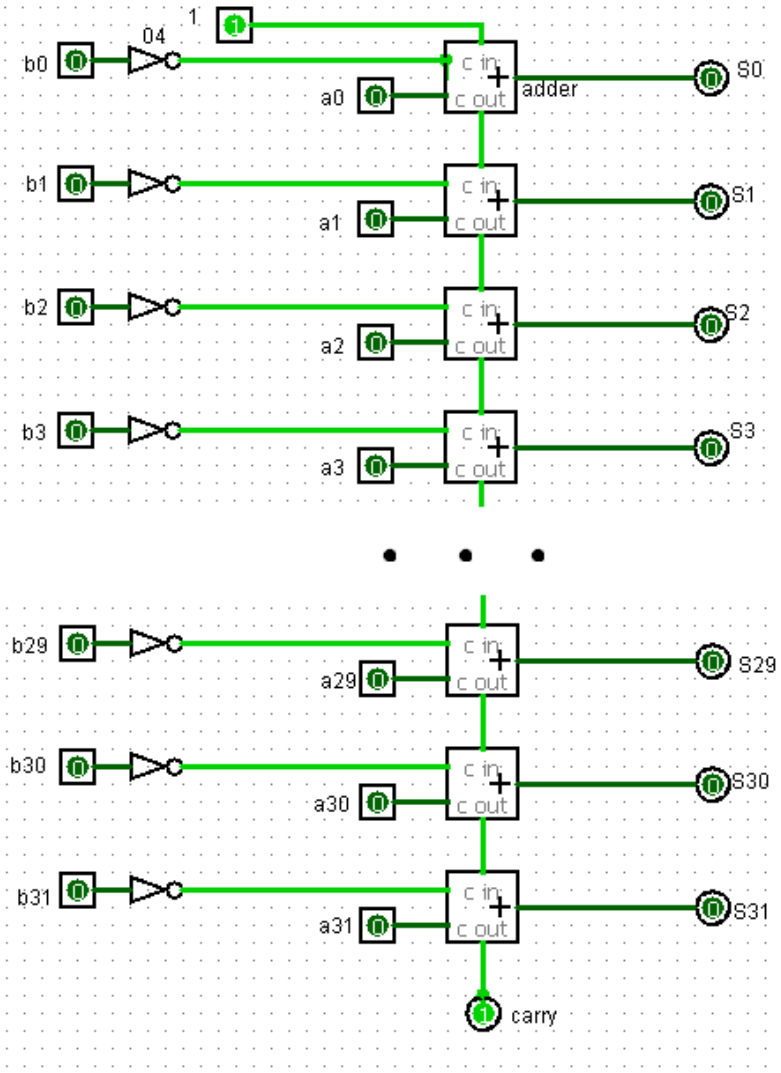
The 2's complement of b is all bits of the binary representation flipped plus one.

We therefore created the following circuit, in which we invert the signal from b and create an adder that takes an input of 1:



Marina Cheng
Sharon Vizcaíno
CSC270 – HW#3

We then simplified the circuit by removing the adder for 1 and instead simply flipped the signals from b and added 1 to the adder that takes the input for a0, thus resulting in the following simplified circuit:



Marina Cheng
Sharon Vizcaíno
CSC270 – HW#3

Problem 2

From the simplified version of problem 1, we noticed that the +1 input for getting the two's complement of b could be used as the switch, since we would only need to add the extra 1 when doing subtraction. Then, instead of always inverting the input of b, it would only need to be inverted when the switch is a 1. The truth table for that would be:

B	switch	output
0	0	0
0	1	1
1	0	1
1	1	0

From this, we noticed that this was equivalent to an XOR gate. This resulted in the following circuit: