

## CSC270 Midterm Exam

This midterm is 70 minutes long. It is closed-books and closed-notes. It is given under the rules of the honor code. All problems are worth the same number of points each.

### Problem 1

Implement  $f = \Sigma(0, 1, 2, 3, 6, 7, 9, 11)$  with

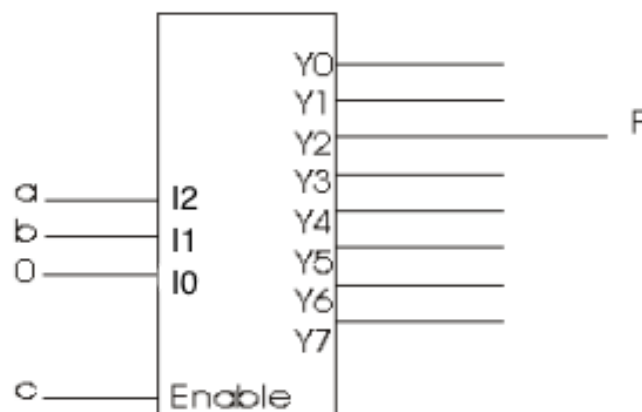
- only NOR gates
- a 3-to-8 decoder with active high outputs and no enable input. You can add any other logic gate needed.
- a 4-to-16 decoder with active low outputs and an active low enable. You can add any other logic gate needed.
- a 4-to-1 multiplexer. You can add any other logic gate needed.

### Problem 2

Implement a fully synchronous (no gating of clock signal, nor use of clear or preset) FSM, with one output that is ON for 1 second, and OFF for 7 seconds. You have available to you one D flip-flop, one JK flip-flop, and one T flip-flop. You have access to any number of decoders, multiplexers, and 2-input and 3-input standard gates.

What clock frequency do you need?

### Problem 3



Implement the function above with an 4-to-1 multiplexer.

## Problem 4

The decoder of Problem 3 is found to have a dead output pin in Y2. Y2 is stuck at 0. It never changes, even if the inputs are set to activate it. Unfortunately we cannot replace the decoder. It's the only one available, and we have to use it. The other 7 outputs work properly, though. Can you rewire the circuit so that we can still implement the function F without adding any new hardware?

## Problem 5

What is the difference between a Moore machine and a Mealy machine? Give an example of both using D flip-flops.

## Problem 6

An FSM with equations  $D0 = Q1$ ,  $D1 = \text{NOT}(Q1 \text{ XOR } Q0)$  is found to have a "*stuck-at*" state, i.e. that it can be stuck in a state and never move to another state. The wanted behavior is for the FSM to evolve through different states, in a cycle.

Correct the design so that the FSM can never be *stuck* in any state. You cannot use the Clear or Preset signal of the flip-flops.