

DM74LS574

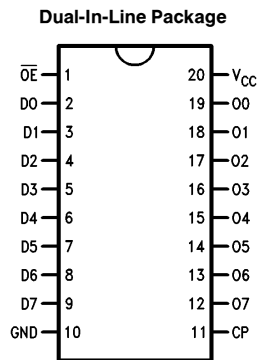
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'LS574 is a high speed low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 'LS374 except for the pinouts.

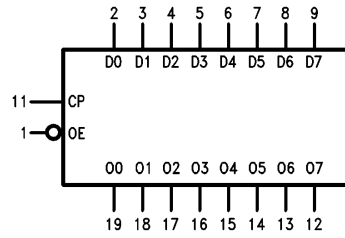
Connection Diagram



TL/F/9815-1

Order Number DM74LS574WM or DM74LS574N
See NS Package Number M20B or N20A

Logic Symbol



V_{CC} = Pin 20
 GND = Pin 10

TL/F/9815-2

DM74LS574 Octal D Flip-Flop with TRI-STATE Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
DM74LS	
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM74LS574			Units
		Min	Nom	Max	
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
I _{OH}	High Level Output Current			-2.6	mA
I _{OL}	Low Level Output Current			24	mA
T _A	Free Air Operating Temperature	0		70	°C
t _s (H)	Setup Time HIGH or LOW	20			ns
t _s (L)	Dn to CP	20			ns
t _h (H)	Hold Time HIGH or LOW	0			ns
t _h (L)	Dn to CP	0			ns
t _w (H)	CP Pulse Width	15			ns
t _w (L)	HIGH or LOW	15			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max, V _{IH} = Min	2.4	3.3		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IL} = Max, V _{IH} = Min		0.35	0.5	V
		I _{OL} = 12 mA, V _{CC} = Min		0.25	0.4	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			-400	μA
I _{OZH}	Off-State Output Current with High Level Output Voltage Applied	V _{CC} = Max, V _O = 2.4V, V _{IH} = Min, V _{IL} = Max			20	μA
I _{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V _{CC} = Max, V _O = 0.4V, V _{IH} = Min, V _{IL} = Max			-20	μA

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit (Note 2) Output Current	$V_{CC} = \text{Max}$	-30		-130	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 3)			45	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Switching Characteristics



$V_{CC} = +5.0V$, $T_A = +25^\circ C$

Symbol	Parameter	$R_L = 2\text{ k}\Omega$, $C_L = 45\text{ pF}$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to On	28		ns
t_{PZH} t_{PZL}	Output Enable Time	28		ns
t_{PHZ} t_{PLZ}	Output Disable Time	20		ns
		25		

Functional Description

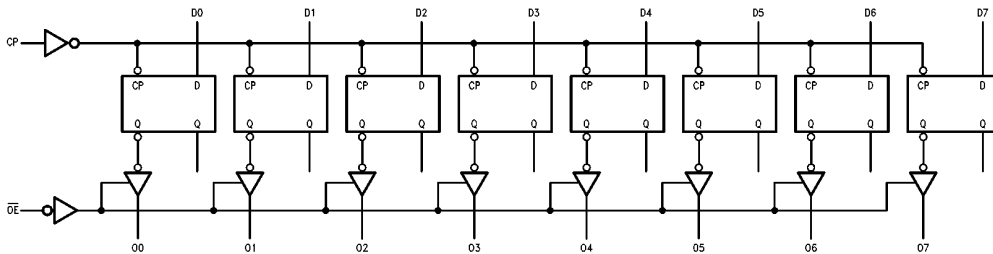
The LS574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Outputs Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Truth Table

Inputs		Outputs	
Dn	CP	OE	On
H		L	H
L		L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

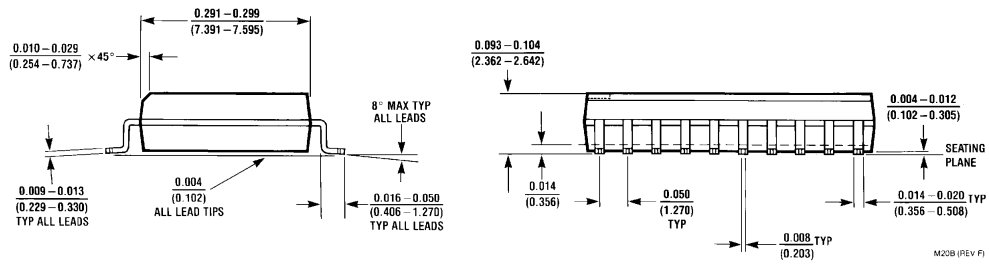
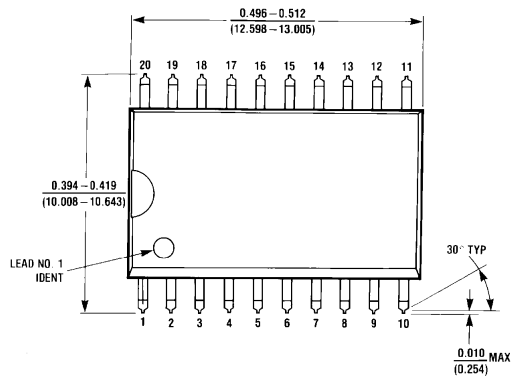
Logic Diagram



TL/F/9815-3



Physical Dimensions inches (millimeters)

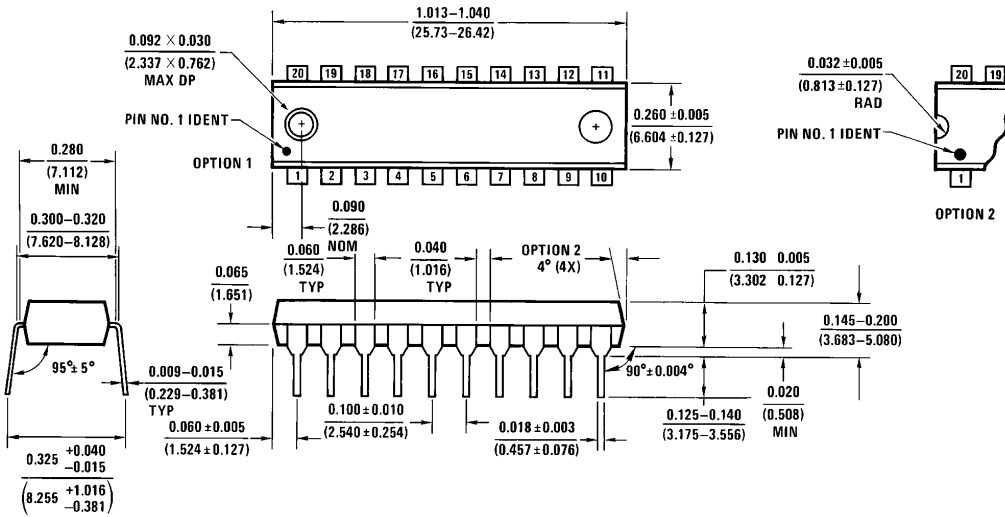


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS574WM
NS Package Number M20B

M20B (REV F)

DM74LS574 Octal D Flip-Flop with TRI-STATE Outputs

Physical Dimensions inches (millimeters)



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS574N
NS Package Number N20A

N20A (REV G)

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