Summary of *Amdahl's Law in the Multicore Era*

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Yang Li

One-sentence summary

In *Amdahl's Law in the Multicore Era*, an article published in 2008 IEEE, M. Hill and M. Marty present a corollary to Amdahl's law for modeling multicore hardware resources and offers insights on improving parallel and sequential performance in future research.

One-paragraph summary

This paper presents a corollary to Amdahl's law for modeling multicore hardware resources. By approximating the speedup of symmetric, asymmetric and dynamic multicore chip based on the corollary, this paper demonstrates the importance of parallelism, chip density and sequential performance in multicore computation. It also encourages desginers to view the entire chip's performance rather than focusing on core efficiencies. Although this hypothetical model is limited by its simplicity and various implementation-wise constraints, it offers insights to stimulates discussion and future research on multicore architecture.

Half-page-summary

This paper presents a corollary that extends Amdahl's law to model the hardware resources for future generations of multicore chips. By approximating the speedup of a variaty of multicore chips with this corollary, it shows important implications on multicore design. It also disscusses limitations of this simple model and provides directions for future research.

The corollary defines a cost model that measures hardware resource in number of Base Core Equivalents (BCE). Moreover, it estimates the sequential performance as a function of the number of BCEs in a core with powerful sequential performance. Amdahl's law is then applied to compute the speed-up as a function of parallel fraction, total number of BCEs and the number of BCEs in a powerful sequetial core.

Three variaties of of multicore chips are discussed in this paper. In a symmetric multicore chip, all cores have the same cost. The speedup model for this type of chips shows that good parallelism, and high performance cores and denser chips are desirable even at a high cost. In an asymmetric chip, one or more cores have more resources and performances than others. The paper demonstrates that asymmetric chips have more speedup potential than symmetric chips. It also ecourages research on speeding sequential performance since denser multicore chips increases the speedup benefit of powerful sequential cores. Finally, in a dynamic multicore chip, parallel cores are dynamically combined to boost the performance of sequential component, using thread-level speculation and helper thread. Although not completely realized, dynamic chips promise a much higher speedup than asymmetric chips do with the same sequential performance.

This paper also disusses limitations of the corollary in real world. Current technology can not fully approximate the hypothetical dynamic chips. Barriers on power, memory and interconnect designs also hinder chips from achiving high performace by increasing resources. On the software side, implementing parallelism and scheduling tasks on complicate multicore chips create notable overhead. Nevertheless, it mentions optimistic opinions that increasing hardware improves performance on problems of large size.

Overall, this paper discusses the speedup potential of multicore chips using Amdahl's law. While making the reader aware of the real world limitations, it stimulates dicussions and future research to make efficient multicore computation realizable.