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February 14, 2011
CSC 270
Lab #3

Lab #3: NAND Gates, Majority Voters and Circuit Decoders

Introduction

The focus of this lab is to explore the universality of the NAND gate, to build a majority voter circuit, and to build and work with circuit decoders.

Materials

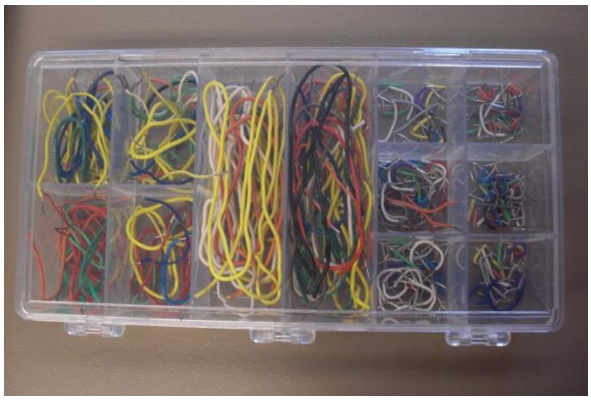

Figure 1. Wiring Kit.

Figure 2. Digital Training Kit.

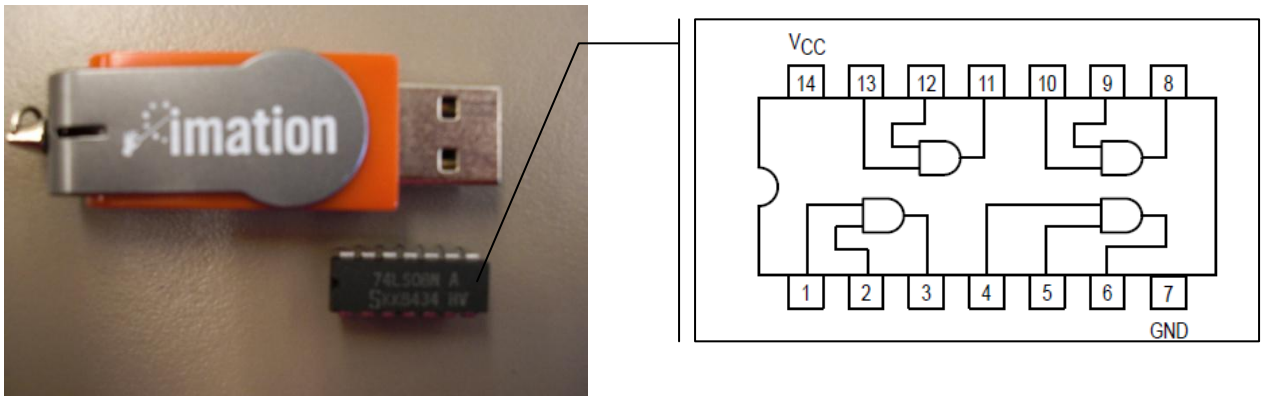

Figure 3. Quad 2-Input AND Gate 74LS08 Compared to a USB Flash Drive.

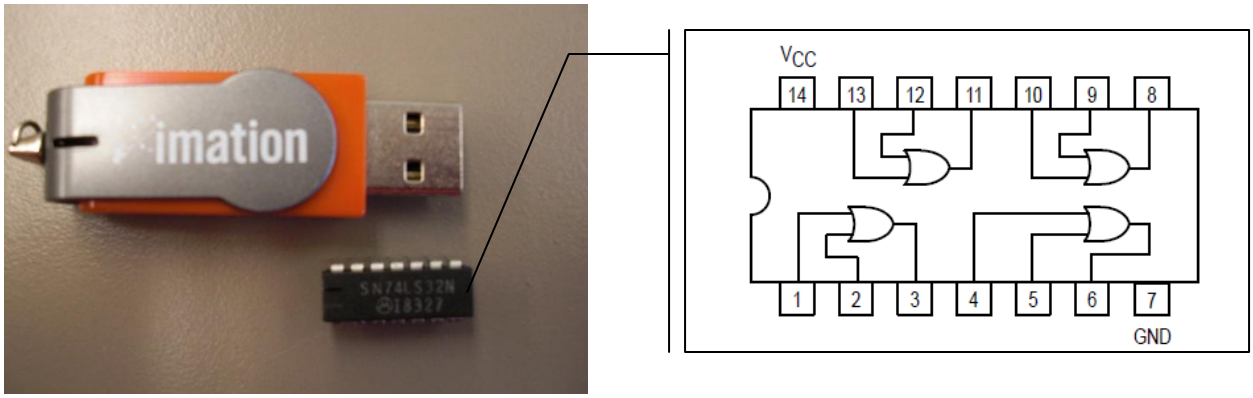

Figure 4. Quad 2-Input OR Gate 74LS32 Compared to a USB Flash Drive.

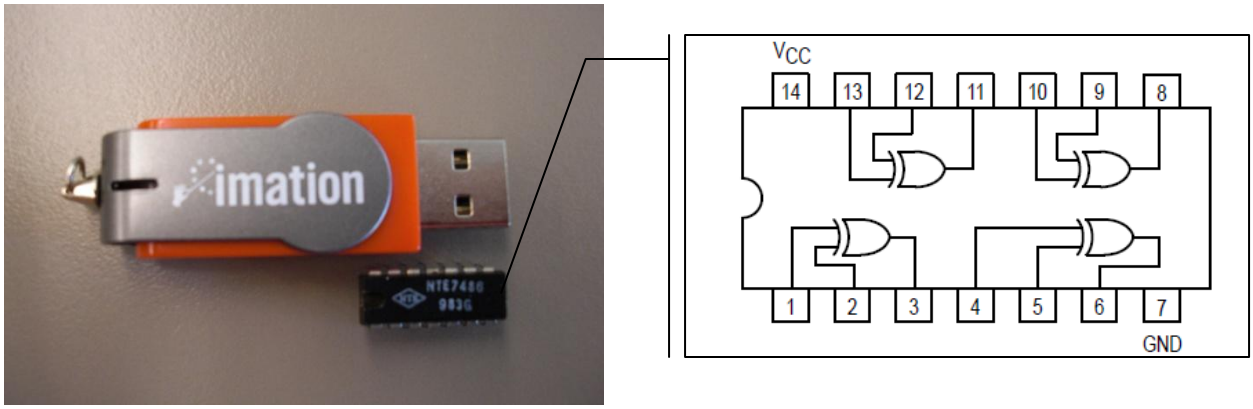

Figure 5. Quad 2-Input XOR Gate 74LS86 Compared to a USB Flash Drive.

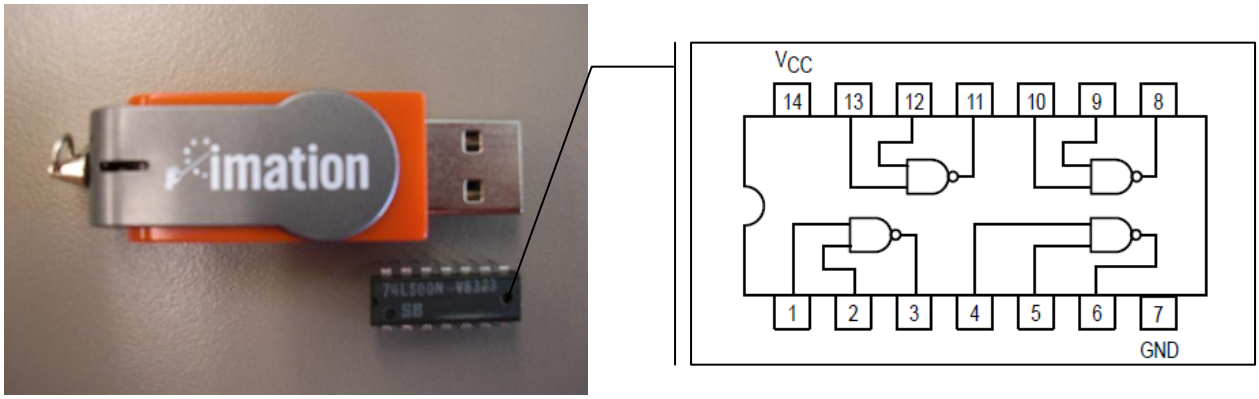

Figure 6. Quad 2-Input NAND Gate 74LS00 Compared to a USB Flash Drive.

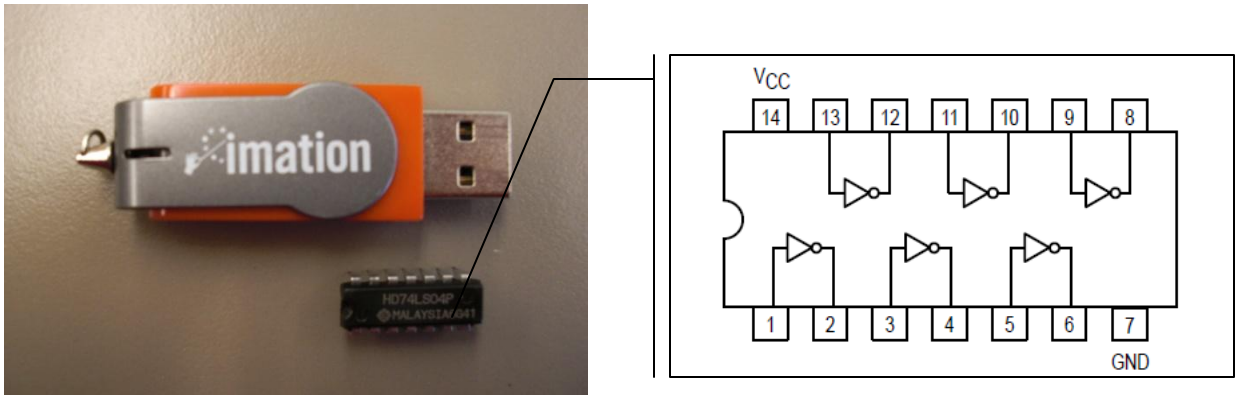

Figure 7. Hex Inverter 74LS04 Compared to a USB Flash Drive.

Universal Gates

In order to prove that a gate is a universal gate, the gate must be able to be used to implement AND, OR, and NOT Boolean functions. For this lab, we will prove that the NAND gates are in fact universal gates by wiring up the basic AND, OR, and NOT functions and the equivalent NAND functions using the Digital Kit and logic gate circuits. Circuits will be deemed equivalent if and only if either both output LED's are on or both output LED's are off all combinations of values (switch on or switch off) for a and b. The following are circuit diagrams used to test the universality of the NAND gate.

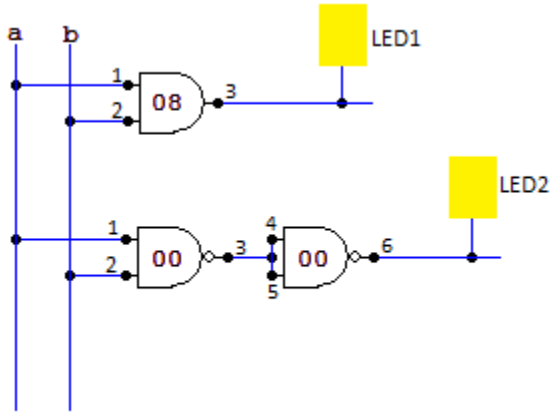

Figure 8. Circuit Diagram to Test a AND b = (a NAND b) NAND (a NAND b).

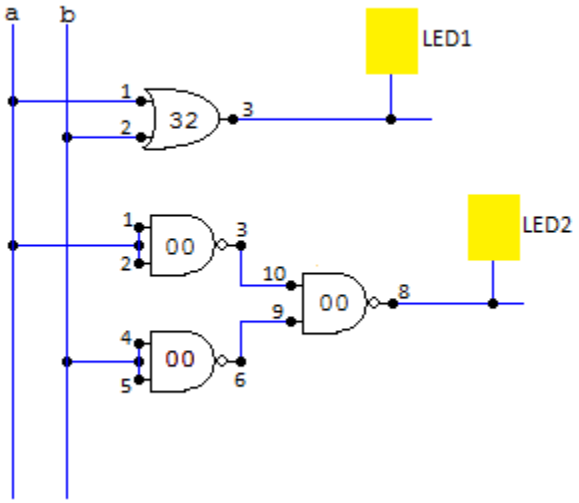

Figure 9. Circuit Diagram to Test a OR b = (a NAND a) NAND (b NAND b).

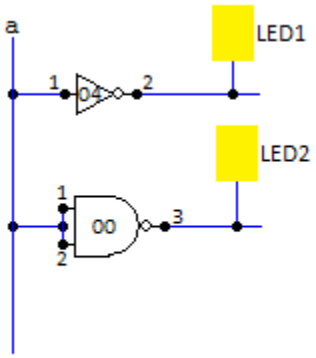

Figure 10. Circuit Diagram to Test NOT a = a NAND a.

When these circuits (Figs. 8-10) were wired up and tested, they confirmed that the NAND gate is in fact a universal gate.

Majority Voter

A majority voter is a circuit that receives and compares 3 inputs. The output of this circuit would then be the majority of the three inputs (output = 1 when 2 or 3 inputs = 1 and output = 0 when 2 or 3 outputs = 0). When one of the inputs is different from the other two, the circuit will output two bits that represent the index of the wrong input (a – 00, b – 01, c – 10, none – 11). To determine which gates to use to build a majority voter, we need to come up with functions for the output (y) and the two bits representing the index of the wrong input (i1 – most significant bit and i0 – least significant bit). To find the function that would yield the simplest circuit, we would have to simplify the functions for y, i1, and i0 using a Karnaugh Map for each.

a	b	c	y	i1	i0
0	0	0	0	1	1
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Table 1. Truth Table for a Majority Voter.

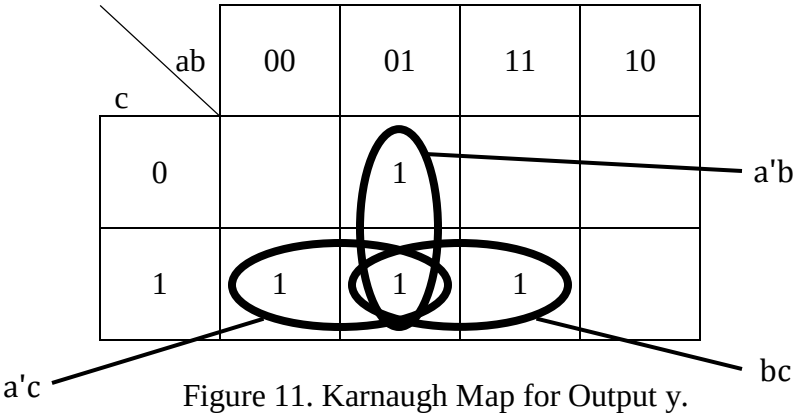

Figure 11. Karnaugh Map for Output y.

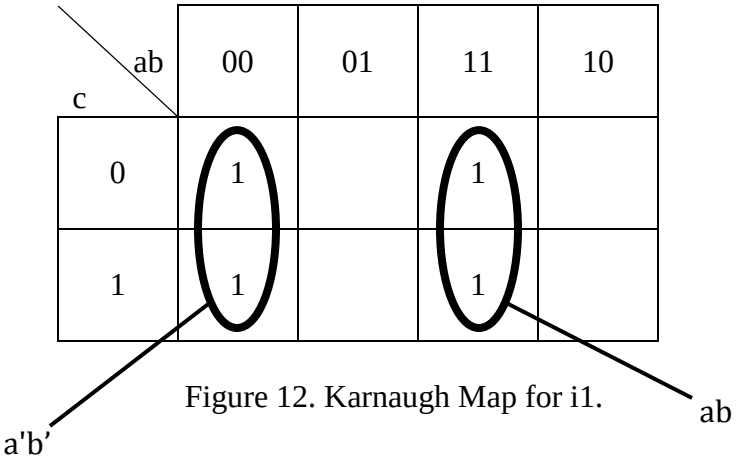

Figure 12. Karnaugh Map for i1.

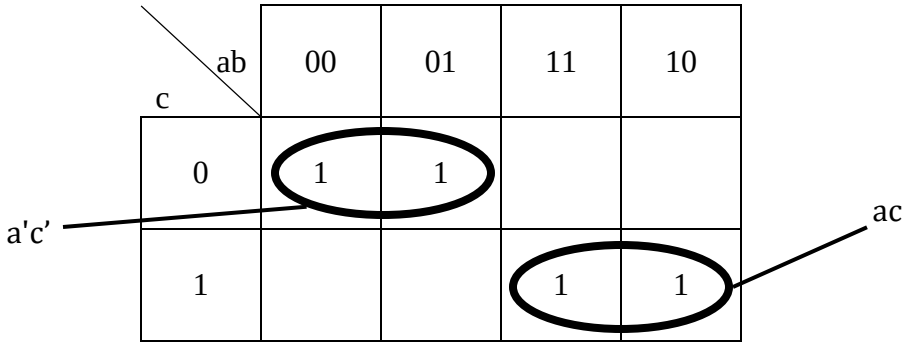

Figure 13. Karnaugh Map for i0.

From these Karnaugh Maps we get y = a·b + b·c + a·c, i1 = a'·b' + a·b = (a⊕b)', and i0 = a'·c' + a·c = (a⊕c)'. Based on this, the following circuit was built:

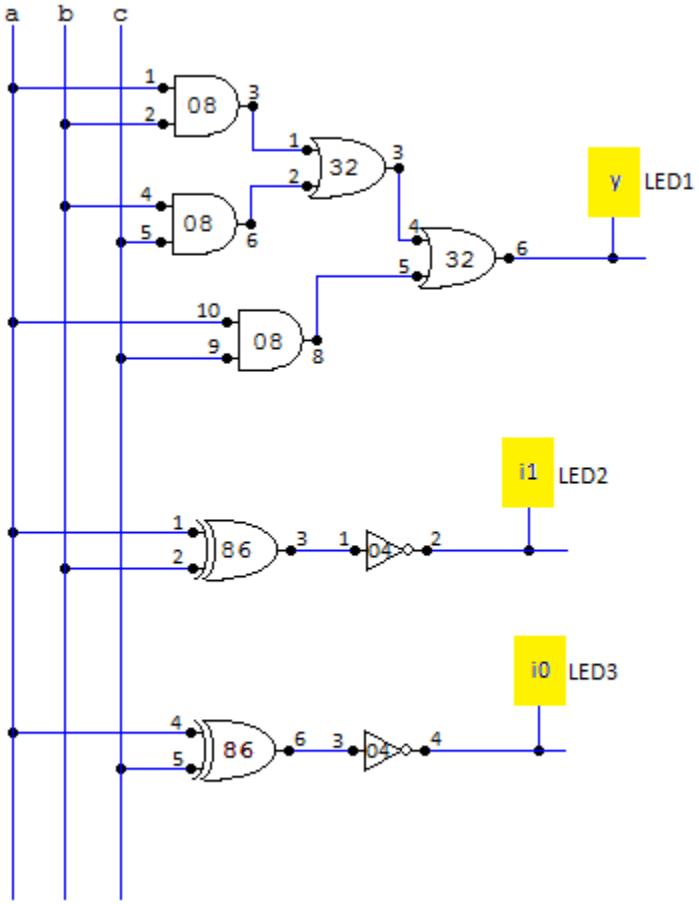

Figure 14. Circuit Diagram for a Majority Voter.

This circuit was verified against a truth table (Fig. 11) for a majority voter and was proven to be the correct implementation for such a circuit.

Decoder Circuit

A decoder circuit decodes the input taking in n inputs and generating 2^n outputs. A decoder with active high outputs would have the following truth table:

b1	b0	y0	y1	y2	y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 2. Truth Table for Decoder that has Active High Outputs.

On the other hand, a decoder with active low outputs would have the following truth table:

b1	b0	y0	y1	y2	y3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Table 3. Truth Table for Decoder that has Active Low Outputs.

The following circuit was implemented on the breadboard section of the Digital Kit (the L's represent LED's):

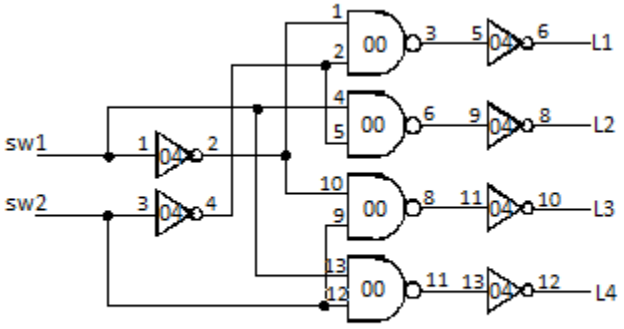

Figure 15. Decoder Implemented with Inverters and NANDs.

When building this circuit, make sure the power is turned off before wiring and verify the connections before turning the power back on. When the circuit was wired correctly, the two inputs were activated and the following truth table was recorded:

sw2 (b1)	sw1 (b0)	L1 (y0)	L2 (y1)	L3 (y2)	L4 (y3)
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 4. Truth Table for the Decoder Circuit (Fig. 15).

Since this truth table matches Table 2, we can conclude that the circuit (Fig. 15) was a decoder with active high outputs.

Next, we connected L1, L2, L3, and L4 to the input of the inverters rather than their output:

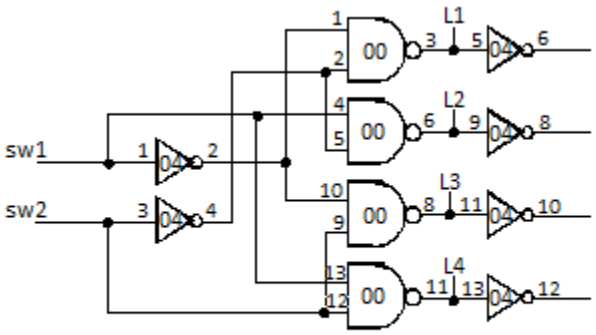

Figure 16. Decoder Implemented with LED's Located at Input of Inverters.

Using this circuit, the following truth table was recorded:

sw2 (b1)	sw1 (b0)	L1 (y0)	L2 (y1)	L3 (y2)	L4 (y3)
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Table 5. Truth Table for the Modified Decoder Circuit (Fig. 16).

Since this truth table matches Table 3, we can conclude that the modified circuit (Fig. 16) was a decoder with active low outputs.

Finally, we worked with the 74LS42 decoder located in Block 6 on the circuit board attached to the Digital Kit. The logic diagram of the circuit is as follows:

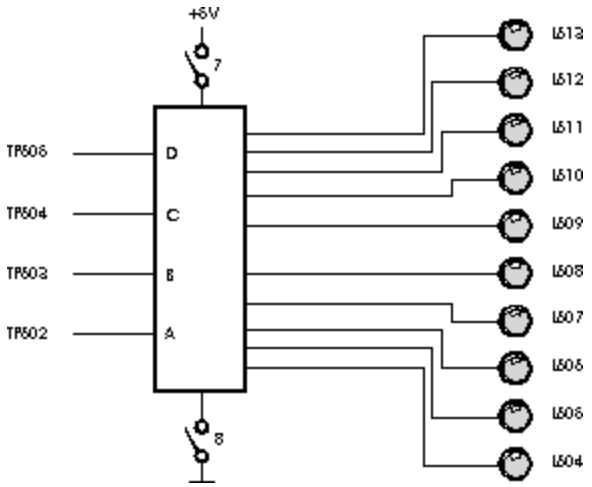

Figure 17. The 7442, as Wired on the HeathKit Digital Trainer.

The four inputs to the 7442 connected to the test points are labeled TP602, TP603, TP604, and TP605. These test points were connected to data switches A, B, C, and D respectively. The ten outputs of the 7442 are connected to 10 LEDs that are labeled L604 to L613. The DIP-switches 7 and 8 must be closed to apply power to the 7442. After turning the Digital Kit on, the data switches were activated and the variations of the output LEDs were recorded in the following table:

A	B	C	D	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 6. Truth Table for the 7442 Decoder.

Since the inactive outputs are all 1, the 7442 decoder is a circuit with active low outputs. Normally, a decoder with n inputs would have 2^n outputs. Thus with 4 inputs we would expect 16 outputs. However, in the case of the 7442 decoder, there are only 10 outputs since it is a 4-to-

10 decoder, thus, all inputs with binary values 0 through 9 have one active output indicated by a 0 (or an LED with light off), whereas all inputs with binary values 10 through 15 have no active outputs (ie. all outputs are 1).